Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.125”**

**ANODE**

**.125”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .125 X .125” DATE: 12/13/22**

**MFG: NAT’L RECTIFIER THICKNESS: .015” P/N: SC125S035A**

**DG 10.1.2**

#### Rev B, 7/19/02